UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/353,847 | 07/15/1999 | HYUN CHANG LEE | 8733/PD-6981 | 4171 |

30827 7590 12/03/2004

MCKENNA LONG & ALDRIDGE LLP
1900 K STREET, NW
WASHINGTON, DC 20006

| EXAMINER | |
|---|---|
| ANYASO, UCHENDU O | |
| **ART UNIT** | **PAPER NUMBER** |
| 2675 | |

DATE MAILED: 12/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) |
|---|---|---|
| | 09/353,847 | LEE ET AL. |
| | Examiner | Art Unit |
| | Uchendu O Anyaso | 2675 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *05 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. **Claims 1-26** are pending in this action.

### *Claim Rejections - 35 USC ' 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 1-26** are rejected under 35 U.S.C. 103(a) as being unpatentable over Moon et al (US Patent 5,793,346) in view of *Tsuchi* (U.S. 5,818,406).

Regarding **independent claims 1, 9, 11** and **19**, and for **claims 4-8** and **10**, Moon teaches a circuit and method of clearing a TFT LCD when the external power is removed from the liquid crystal display (column 1, lines 6-12).

Furthermore, Moon teaches a liquid crystal display device, comprising a plurality of data lines, a plurality of thin-film transistor (TFT) liquid crystal display cells electrically coupled to said plurality of data lines and arranged as a first string of TFT display cells electrically coupled together by a first gate line and a second string of TFT display cells electrically coupled together by a second gate line, said second string of TFT display cells comprising respective support capacitors therein electrically coupled to said first gate line (column 4, lines 37-48).

Furthermore, Moon teaches a screen clearing circuit 40 connected at an input to the gate driving circuit 10 wherein the controller 30 controls gate driving circuit 10, which supplies gate

on/off voltages sequentially through the gate lines to the thin film transistors 70 (column 4, lines 12-23, figure 6 at 10, 30).

Furthermore, the gate on/off generator 50 generates the Voff and Von voltages which are sent to the gate lines by the gate driving circuit 10 (column 4, lines 23-25, figure 6 at 10, 50) wherein the screen clearing circuit 40 is connected to the Voff output of gate on/off generator 50 (column 4, lines 25-26). When the external power is disconnected, the screen clearing circuit 40 operates to discharge the storage capacitors 80 connected to the gate lines (column 4, lines 27-29). Elimination of the residual image improves the quality of TFT LCDs (column 4, lines 33-34). This invention may be used in a wide variety of display devices such as notebook computers, handheld devices, and flat panel television screens (column 4, lines 33-36).

However, Moon does not teach a level shifting means for receiving a power supply voltage and a ground voltage to apply a first voltage level for turning off the TFTs to the gate lines upon power-on and to apply a higher voltage than the ground voltage to the gate lines upon power-off. On the other hand, Tsuchi teaches a driver circuit for a LCD device (column 1, lines 5-9) wherein a level shifter 70c receives power supply (figures 7, 13 at 15c, 20c) via a high voltage system and a ground voltage via a low voltage system (see figure 7 & 13) such that figure 15 teaches how a first voltage level is employed for turning off the transistors upon power-on (column 8, lines 44-64, figures 14 & 15) and figures 8-11 teaches how a higher voltage level than ground voltage (i.e., 5V) is applied to the transistors upon power off (column 8, lines 14-35, figures 9-12).

Thus, it would have been obvious to a person of ordinary skill in the art to combine Moon and Tsuchi because while Moon teaches the concept of clearing a TFT LCD when the external

power is removed from the liquid crystal display (column 1, lines 6-12), Tsuchi teaches a driver circuit for a LCD device (column 1, lines 5-9) wherein a level shifter 70c receives power supply (figures 7, 13 at 15c, 20c) via a high voltage system and a ground voltage via a low voltage system (see figure 7 & 13) such that figure 15 teaches how a first voltage level is employed for turning off the transistors upon power-on (column 8, lines 44-64, figures 14 & 15) and figures 8-11 teaches how a higher voltage level than ground voltage (i.e., 5V) is applied to the transistors upon power off (column 8, lines 14-35, figures 9-12). The motivation for combining these inventions would have been to provide a driver circuit for a liquid crystal display device employing a data line driver circuit for a digital signal input and a digital signal output, which can accurately output a power source voltage with a simple circuit construction (column 2, lines 29-33).

Regarding **claims 2** and **3,** in further discussion of claim 1, Moon teaches how the first voltage level has a lower voltage level than a minimum value of the image signals (*see* figure 5; *see also* Abstract).

Regarding **claims 12-18, 20-26,** in further discussion of claims 11 and 19, Moon teaches an invention that comprises a capacitor of which one end is connected to the external power; a diode of which the anode is connected to the other end of said capacitor, and the cathode is grounded; and a PMOS transistor of which the gate electrode is connected to the anode of said diode and the other end of said capacitor, the source electrode is grounded, and the drain electrode is connected to one end of a support capacitor of a TFT LCD (column 2, lines 10-27).

Furthermore, Moon teaches a means for detecting whether external power has been shut off; charging the support capacitor if the external power is not shut off, and then returning to the first detecting step; discharging the support capacitor if the external power is shut off, and then returning to the first detecting step (column 2, lines 28-35).

***Response to Arguments***

**4.** Applicant's arguments with respect to claims 1-26 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

**5.** The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent 5,680,064 to *Masaki et al* for a level converter for CMOS 3V to from 5V.

U.S. Patent 5,414,443 to Kanatani et al a drive device for driving a matrix-type LCD apparatus.

***Contact Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Uchendu O. Anyaso whose telephone number is (703) 306-5934. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steve Saras, can be reached at (703) 305-9720.

**Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

Washington, D.C. 20231

**or faxed to:**

**(703) 872-9314 (for Technology Center 2600 only)**

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Uchendu O. Anyaso

11/29/2004

CHANH NGUYEN
PRIMARY EXAMINER